Trigger in and trigger out port

2016.2.24

Revision history

Date	Version	Revision
2012-9-25	1.1	 Modify the section 4 -Waveform of the trigger out on pin3; former waveform is one pulse for every subframe, now it is one pulse every frame. Pulse width is about 40us. Add PWM output on pin led0;
2012-9-21	1.0	Initial version

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1. Connector for trigger in and out

For W 4100 2012-2-21 PCB: Connector J6

For Faro PCB: Connector J1.

The connector is same for both PCB. The connector is a 10 pin SMT connector. Schematic diagram of the connector is as following.



picture 1 Schematic diagram of connector of trigger

2. Pin functions of the trigger connector

Pin1:	2.5V power	
Pin2 :	triger signal output.	High: 2.1V-2.5V; low: 0V-0.4V.
Pin3:	triger signal input.	low to high edge is one trigger. High: 1.7-2.5V; Low: 0-0.7V
Pin4:	信号发生器	
Pin10:	GND	

3. The position of the connector on PCB

For W4100 2012-2-21, the connector J6 is on the upper left of the PCB. The upper pin is pin1.





For FARO PCB. The connector J1's position is as the following image. The left pin is pin1.

picture 2 position of J1 on FARO PCB

4. Waveform of the trigger out on pin3

On pin3 of the connector, trigger output is one pulse for every frame. Pulse width is about 40us. The waveform is as picture3. On the picture, channel 1 is the trigger output waveform which is one pulse per frame; channel 2 is the subframe's trigger signal, one pulse per subframe.

Note: Subframe is also called bit frame. For example, one 8-bit gray picture frame includes 8 subframes. All the most significant bit composes the most significant subframe.



subframe trigger out)

5. PWM output

PWM output pin is the pin4 of J1 on FARO PCB(J6 on W 4100 2012-2-21 PCB) as well as pin C33(FPGA_PWM) of the V5 FPGA as picture 8 .

Note:User should remove R305 and solder R306, as picture 4 Net FPGA_PWM to LED_PWM.



picture 4 Net FPGA_PWM to LED_PWM

Net LED_PWM is buffered by U35 as picture 5 , LED_PWM_BUF is output from Pin7 of J19 as picture 6

		100NF-0603SMT	C242
LED_ENABLE 1	U35 A1 Y1	<u>6 LED_ENABLE_BU</u> F	
2	GND VCC	5	
LED_PWM 3	A2 Y2	4 LED_PWM_BUF Note: Pullups on	LED board

picture 5 LED_PWM is buffered by U35, LED_PWM_BUF is output



picture 6 LED_PWM_BUF and LED_ENABLE_BUF are output from J66

PWM output is constant period. Period is 40us. It has 32 level, 0-31. Number 0's duty circle is least and number 31's duty circle is highest.

connect device] 🗟						
DmdType Frame Rate Gray	XGA_07A 10000 Hz 8 V Bit		Open	Multi Files			
Output Sync I	ne, WLP_TRIGGER_SIM		Tr	igger			
COMP_D	ATA INS_FLIP	PWM Duty	Cycle:		trol: ON / OFF		
	Control thi (0-31),PWM		Start	St	op	Exit	

picture 7 SDK control panel

The PWM waveform is also output to the LED(D3) as picture 10. thus when control the

PWM value, the PWM duty circle will be modified. The LED(D3)'s luminance will change.

6. LED ON/OFF

LED ON/OFF is output from pin B33 of V5 FPGA as picture8. Net name is LED_ENABLE_WIN.

02	2D		
	3.3V	B32	
20 2 20 2	IO_L0P_11 IO_L0N_11	A33	
32 - 3	IO_L1P_11	B33 C33	LED ENABLE WIN LED ENABLE WIN 18
	IO_L1N_11 IO_L2P_11	C32	FPGA_PWM 18
	IO_L2N_11	D32 C34	
	IO_L3P_11 IO_L3N_11	D34	FPGA_GPIO_A0 J22
22 2	IO_L4P_11	G32 H32	EPGA GPIO A2
	IO_L4N_VREF_11 IO_L5P_11	F33	6
	IO L5P 11	E34 E32	
	IO_L6P_11	E33	. X
8 8	IO_L6N_11 IO_L7P_11	G33 F34	
10 - 1	IO_L7N_11	J32 ×	

picture 8 FPGA's PWM and LED control pins

LED_ENABLE_WIN is multiplexed by U38 as picture 9. Output net name is LED_ENABLE.



picture 9 multiplex the LED_ENABLE

Note: User should connect pin6 of U30 to GND

LED _ENABLE is buffered by U35 as picture 5. Output net name is LED_ENABLE_BUF LED_ENABLE_BUF is output from pin1 of J19 as picture 6.

LED_ENABLE_WIN waveform is also output to the LED(D4) as picture 10. thus when control the LED ON/OFF, D4 will on or off.



picture 10 LED D3 display PWM waveform and LED D4 display LED ON/OFF waveform